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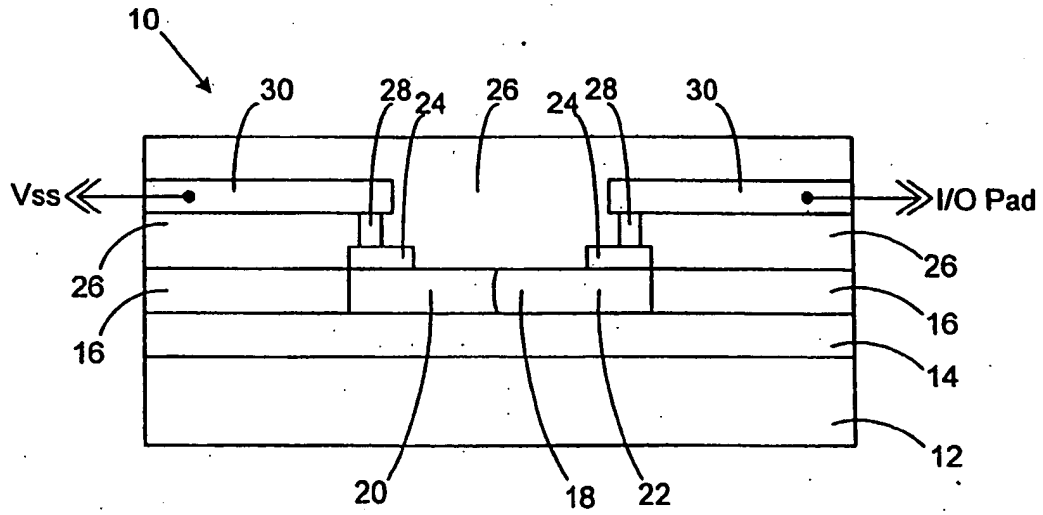

(57) Abstract: A silicon-on-insulator (SOI) diode (10). The SOI diode (10) has an active region (18) having an anode (20) disposed adjacent a cathode (22); a first silicide layer (24) formed on the anode (20) distal a junction between the anode (20) and the cathode (22) and a second silicide layer (24) formed on the cathode (22) distal the the junction between the anode (20) and the cathode (22); and an oxide layer (26) isolating the first and second silicide layers (24). Also disclosed is a method of fabricating the SOI diode (10).

WO 02/061841 A2

SALICIDE BLOCKED DIODE AND METHOD OF MANUFACTURE

TECHNICAL FIELD

The present invention generally relates to the manufacture of semiconductor devices, and, more specifically, relates the manufacture of a silicon-on-insulator (SOI) diode having a salicide blocked region, the diode being particularly well suited for use as an electrostatic discharge (ESD) protection device.

BACKGROUND ART

Traditional silicon-on-insulator (SOI) diodes are typically manufactured by using a polysilicon layer, or poly layer, to define an unsilicided region. There are, however, several shortcomings associated with such a conventional diode. The foregoing poly-defined diode exhibits a relatively high resistance (e.g., 500 ohm-μm to 2,000 ohm-μm) which adversely affects diode performance, especially when used as an electrostatic discharge (ESD) protection device. The high resistance is a result of low doping in the active region, especially in the areas directly below the gate oxide and poly layers as these layers tend to impede dopant penetration into the active region. In addition, a gate oxide layer, disposed on the active region, is susceptible to voltage overstress and may become damaged during diode operation.

DISCLOSURE OF THE INVENTION

According to one aspect of the invention, the invention is a silicon-on-insulator (SOI) diode. The SOI diode has an active region having an anode disposed adjacent a cathode; a first silicide layer formed on the anode distal a junction between the anode and the cathode and a second silicide layer formed on the cathode distal the junction between the anode and the cathode; and an insulating layer isolating the first and second silicide layers.

According to another aspect of the invention, the invention is a silicon-on-insulator (SOI) diode. The SOI diode has an active region having an anode and a cathode; a first silicide layer formed on the anode distal a junction between the anode and the cathode and a second silicide layer formed on the cathode distal the junction between the anode and the cathode; and a resistor-protect mask formed on a central region of the active layer and defining the placement of the silicide layer.

According to yet another aspect of the invention, the invention is a method of fabricating a silicon-on-insulator (SOI) diode. The method includes the steps of (a) defining an active region on an SOI wafer; (b) implanting a first portion of the active region with dopant to form an anode and implanting a second portion of the active region with dopant to form a cathode; (c) depositing a resistor-protect mask on a central region of the active region, the resistor-protect mask defining silicide regions; and (d) forming a silicide layer in the silicide regions defined by the resistor-protect mask.

BRIEF DESCRIPTION OF DRAWINGS

These and further features of the present invention will be apparent with reference to the following description and drawings, wherein:

FIG. 1 is a cross-section of a salicide blocked diode arranged as an electrostatic discharge (ESD) protection device;

FIG. 2 is a flow diagram of a method of manufacturing the salicide blocked diode;

FIG. 3a is a cross-section of the salicide blocked diode in a first intermediate stage of manufacture;

FIG. 3b is a cross-section of the salicide blocked diode in a second intermediate stage of manufacture;

FIG. 3c is a cross-section of the salicide blocked diode in a third intermediate stage of manufacture;

FIG. 3d is a cross-section of the salicide blocked diode in a fourth intermediate stage of manufacture;

FIG. 3e is a cross-section of the salicide blocked diode in a fifth intermediate stage of manufacture; and

FIG. 3f is a cross-section of the salicide blocked diode in a last stage of manufacture.

MODES FOR CARRYING OUT THE INVENTION

In the detailed description which follows, identical components have been given the same reference numerals, regardless of whether they are shown in different embodiments of the present invention. To illustrate the present invention in a clear and concise manner, the drawings may not necessarily be to scale and certain features may be shown in somewhat schematic form.

Referring to FIG. 1, a salicide blocked diode 10 is illustrated. The diode 10 is formed on a silicon-on-insulator (SOI) integrated circuit having a silicon substrate 12, a buried oxide (BOX) layer 14 formed on the substrate 12 and a silicon layer (also referred to as an active layer) disposed on the buried oxide layer 14. Within the silicon layer, shallow trench isolation (STI) regions 16 define the placement of silicon active regions, one of the active regions being used for the diode 10 and is referred to as active region 18. The active region 18 has a P+ region, or anode 20, and an N+ region, or cathode 22. A silicide layer 24 (also known in the art as a salicide structure) is formed on the anode region 20 distal to the P+ region and N+ region interface, or P-N junction. Another silicide layer 24 is deposited on the cathode region 22 distal to the P-N junction. As is known in the art, the silicide layers 24 establish conduction to the anode region 20 and the cathode region 22. One or more insulating layers, such as oxide layer 26, are formed to isolate the active areas of the diode 10. Contacts 28 and metal layers 30 are formed in the oxide 26 to respectively establish electrical connection to the anode 20 and the cathode 22 through the silicide layers 24.

The diode 10 can be used for a variety of purposes, including use as an electrostatic discharge (ESD) protection device. For example, the cathode 22 can be coupled via the silicide layer 24 and respective contact 28 and metal layer 30 to an I/O pad, or other node, to be protected. In this arrangement the anode 20 is connected to ground, or Vss, via the anode's respective silicide layer 24, contact 28 and metal layer 30. In another arrangement the anode 20 is coupled to the I/O pad and the cathode 22 is coupled to a supply voltage, or Vdd (not shown).

Both the P+ region and N+ region are heavily doped (e.g., about 10^{18} atoms/cm^2 to about 10^{22} atoms/cm^2) to give the diode 10 a relatively low resistance (e.g., about 100 ohm-μm to about 300 ohm-μm) which forward biases at a relatively low bias voltage (e.g., about 0.3 volts to about 0.6 volt) and breaks down at a relatively low reverse break down voltage (e.g., about 3 volts to about 4 volts), thereby exhibiting traits important for good ESD protection.

Referring now to FIG. 2, a method 40 is illustrated in flowchart format for manufacturing the diode 10 illustrated in FIG. 1. The method 40 starts in step 42 in which an SOI wafer is manufactured. With additional

reference to FIG. 3a, the SOI wafer, or SOI material, has the silicon substrate 12 having the buried oxide layer 14 disposed thereon. A silicon layer 44 (or active layer) is disposed on the buried oxide layer 14 in conventional format. The SOI arrangement illustrated in FIG. 3a is manufactured using conventional techniques.

Next, in step 46, and as illustrated in FIG. 3b, the active region 18 is defined in the silicon layer 44 by fabricating shallow trench isolation (STI) regions 16 using conventional techniques.

The P+ region, or anode 20, is formed in the active region in step 48 and as further illustrated by FIG. 3c. More specifically, the P+ region is defined by depositing a P+ mask 50 over areas where exposure to P+ implantation should be minimized, such as the future N+ region of the active region 18 and adjacent STI 16. Next, the device is doped using standard PMOS source/drain implants, such as on the order of about 10^{18} atoms/cm^2 to about 10^{20} atoms/cm^2, thereby forming the anode 20. Subsequently, the P+ mask is stripped from the device in step 52. The P+ implantation step may be used to simultaneously dope other areas of the wafer in the fabrication of other devices.

In similar fashion, the N+ region, or cathode 22, is formed in the active region 18 in step 54 and as further illustrated by FIG. 3d. More specifically, the N+ region is defined by depositing an N+ mask 56 over the P+ region, or anode 20, and adjacent STI 16. Next, the device is doped using standard NMOS source/drain implants, such as on the order of about 10^{18} atoms/cm^2 to about 10^{20} atoms/cm^2, thereby forming the cathode 22. The N+ implantation step may be used to simultaneously dope other areas of the wafer in the fabrication of other devices.

It is noted that, openings in the N+ and P+ masks should overlap with each other by at least the tolerance, or error margin in placement, of the mask to ensure that there is no undoped region in the area of a P-N junction 58 formed at the interface of the P+ region and the N+ region. As mentioned, the N+ and P+ regions are implanted using standard NMOS and PMOS source/drain implants, respectively. Other implants, such as extension and halo implants, may or may not be blocked as is desired for the anticipated function of the diode 10 being manufactured. Subsequent to the N+ doping, the N+ mask is stripped from the device in step 60. As one skilled in the art will appreciate, the active region 18 can be doped with N+ implants prior to being doped with P+ implants thereby reversing pairs of steps 48/52 and 54/60.

After the active region 18 has been doped, the regions for silicidation are defined by depositing a resistor-protect (RSPT) mask 62 in step 64 and as illustrated in FIG. 3e. It is noted that salicidation is taken herein to have the same meaning as silicidation. The RSPT mask 62 is placed in all regions where silicide is not desired. More specifically, the RSPT mask 62 is placed over the P-N junction 58 and extends over the P+ region and the N+ region to block the deposition of silicide over the desired active portions of the N+/P+ function. The area masked by the RSPT mask 62 is selected to result in a desired resistance of the diode 10 since, as the size of the silicide layers 24 increases, the resistance of the diode decreases. It should be appreciated that the RSPT mask 62 is used to block the silicide layers 24 from the central junction region of the active region 18, but the silicide layers 24 is allowed to form on the distal areas of the anode 20 and cathode 22, respectfully, to provide conduction to other devices as described in greater detail above. RSPT mask 62 is also deposited over the STI regions 16 to prevent silicide formation on the STI regions 16. The RSPT mask 62, typically an oxide, is conventionally used to define resistors formed on the wafer and is therefore typically a part of existing steps in

most overall wafer fabrication processes. Accordingly, the RSPT mask 62 used for the salicide blocking function is deposited using the conventional techniques used when defining resistor elements.

Once the RSPT mask 62 is formed to define the silicide regions, the silicide layers 24 are formed in step 66 using conventional techniques. More specifically, silicide is formed depositing metal in at least the unmasked areas and reacting the metal with the exposed silicon areas of the anode 20 and cathode 22. Preferably, a $TiSi_2$ (titanium) salicide process is employed, although $CoSi_2$ (cobalt), $PtSi_2$ (platinum) and $MoSi_2$ (molybdenum) salicide processes may also be used. Next, the RSPT mask 62 is stripped in step 68 using conventional techniques.

Subsequently, the oxide material 26, the contacts 28 and the metal layers 30 are formed using conventional techniques in order to protect the diode 10, isolate the two silicide layers 24 and couple the diode 10 to other devices or nodes as is desired. The formation of the oxide material 26, the metal layers 30 and the contacts 28 are completed in step 70 and shown in an exemplary formation in FIG. 3f.

Although particular embodiments of the invention have been described in detail, it is understood that the invention is not limited correspondingly in scope, but includes all changes, modifications and equivalents coming within the spirit and terms of the claims appended hereto.

CLAIMS

What is claimed is:

1. A silicon-on-insulator (SOI) diode (10), comprising:

an active region (18) having an anode (20) disposed adjacent a cathode (22);

a first silicide layer (24) formed on the anode (20) distal a junction between the anode (20) and the cathode (22) and a second silicide layer (24) formed on the cathode (22) distal the junction between the anode (20) and the cathode (22); and

an insulating layer (26) isolating the first and second silicide layers (24).

2. The SOI diode (10) according to claim 1, wherein placement of the first and second silicide layers (24) is defined by a resistor-protect mask (62).

3. The SOI diode (10) according to claim 1, wherein the anode (20) and the cathode (22) are respectively implanted with P+ and N+ dopant before deposition of a mask (62) to define placement of the first and second silicide layers (24).

4. The SOI diode (10) according to claim 1, wherein the anode (20) and the cathode (22) are respectfully coupled to external nodes such that the SOI diode (10) is configured as an electrostatic discharge protection device.

5. The SOI diode (10) according to claim 1, wherein the SOI diode (10) has a resistance of about 100 ohm-μm to about 300 ohm-μm.

6. A method of fabricating a silicon-on-insulator (SOI) diode (10), comprising the steps of:

(a) defining an active region (18) on an SOI wafer;

(b) implanting a first portion of the active region (18) with dopant to form an anode (20) and implanting a second portion of the active region (18) with dopant to form a cathode (22);

(c) depositing a resistor-protect mask (62) on a central region of the active region (18), the resistor-protect mask (62) defining silicide regions; and

(d) forming a silicide layer (24) in the silicide regions defined by the resistor-protect mask (62).

7. The method according to claim 6, wherein step (b) is carried out before step (c).

8. The method according to claim 6, further comprising the step of respectively coupling the anode (20) and the cathode (22) to external nodes such that the SOI diode (10) is configured as an electrostatic discharge protection device.

9. The method according to claim 6, further comprising the step of stripping the resistor-protect mask (62) following silicide formation.

10. The method according to claim 6, wherein the central area having the resistor protect mask (62) is selected to result in the SOI diode (10) having a resistance of about 100 ohm-µm to about 300 ohm-µm.

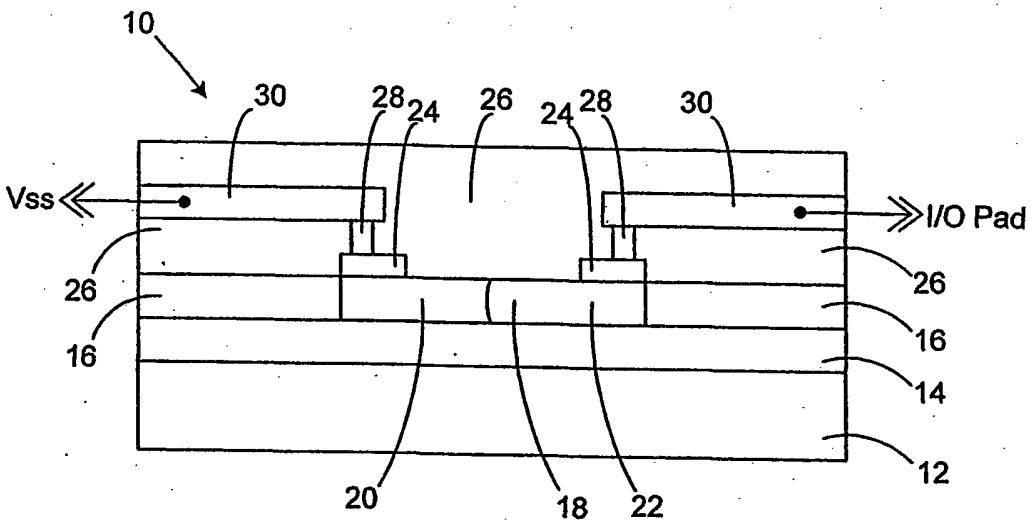

FIG. 1

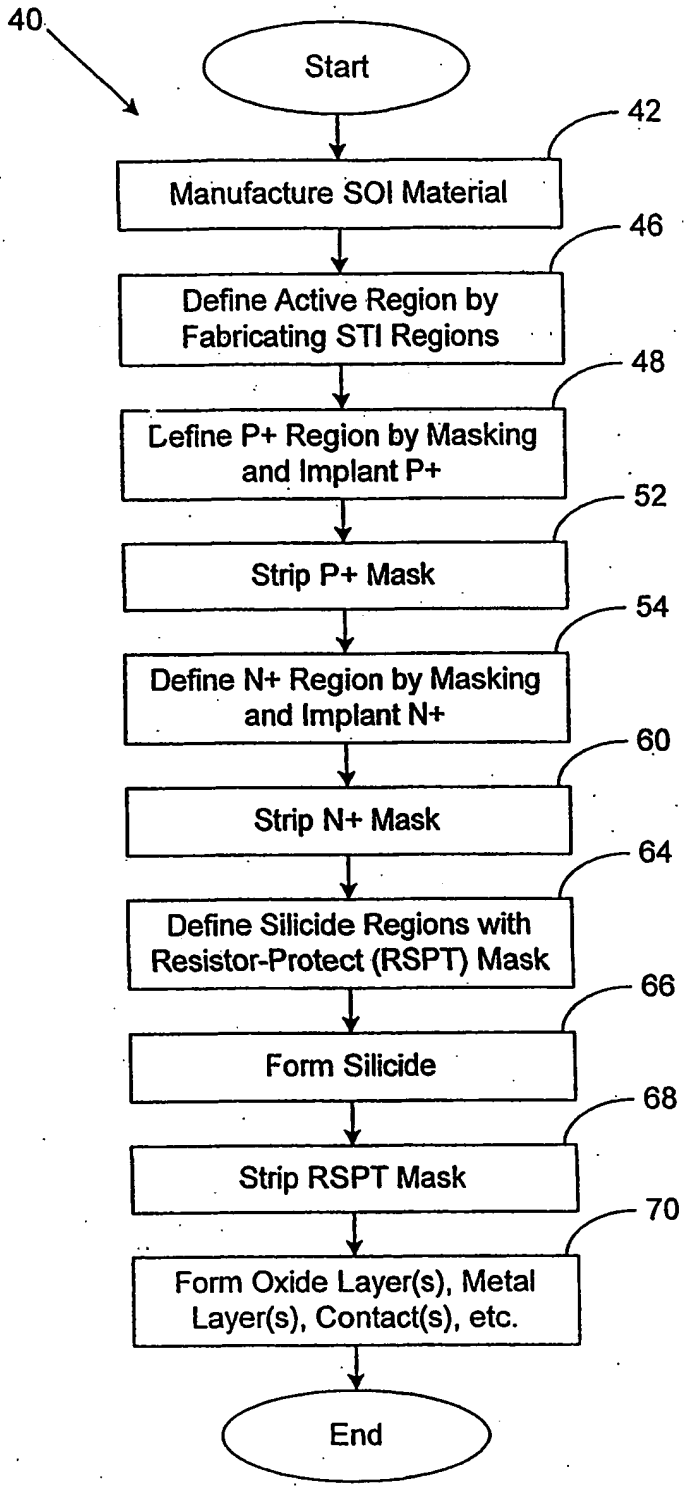
40
Start
42
Manufacture SOI Material
46
Define Active Region by Fabricating STI Regions
48
Define P+ Region by Masking and Implant P+
52
Strip P+ Mask
54
Define N+ Region by Masking and Implant N+
60
Strip N+ Mask
64
Define Silicide Regions with Resistor-Protect (RSPT) Mask
66
Form Silicide
68
Strip RSPT Mask
70
Form Oxide Layer(s), Metal Layer(s), Contact(s), etc.
End

FIG. 2

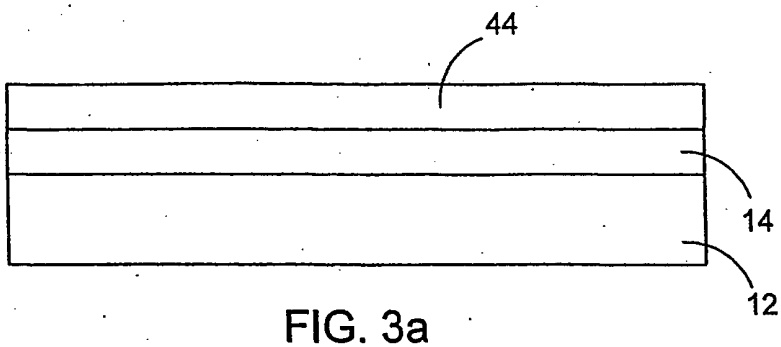

FIG. 3a

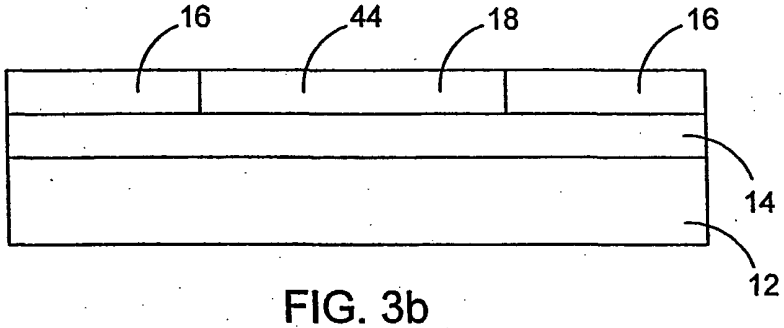

FIG. 3b

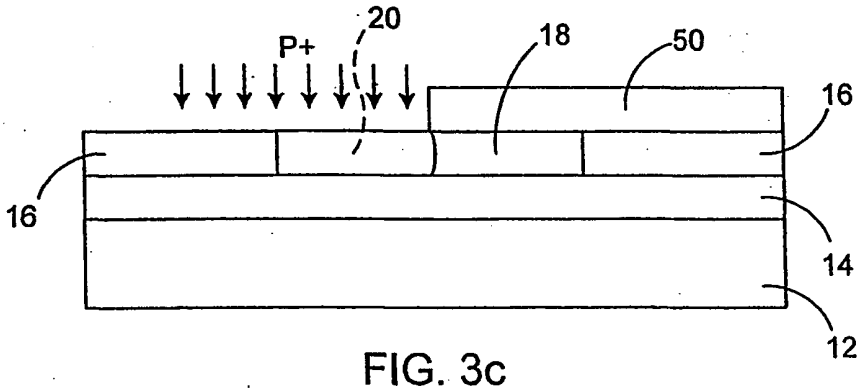

FIG. 3c

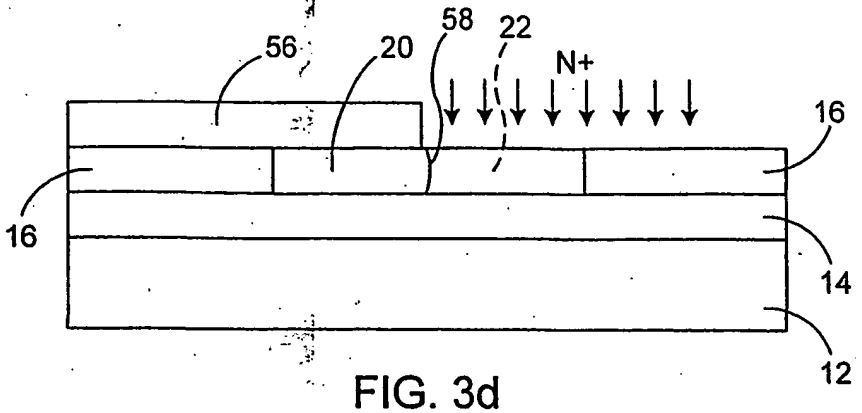

FIG. 3d

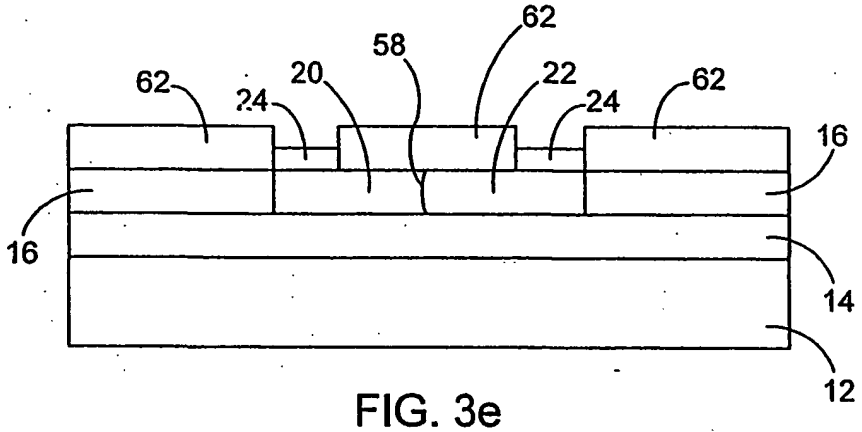

FIG. 3e

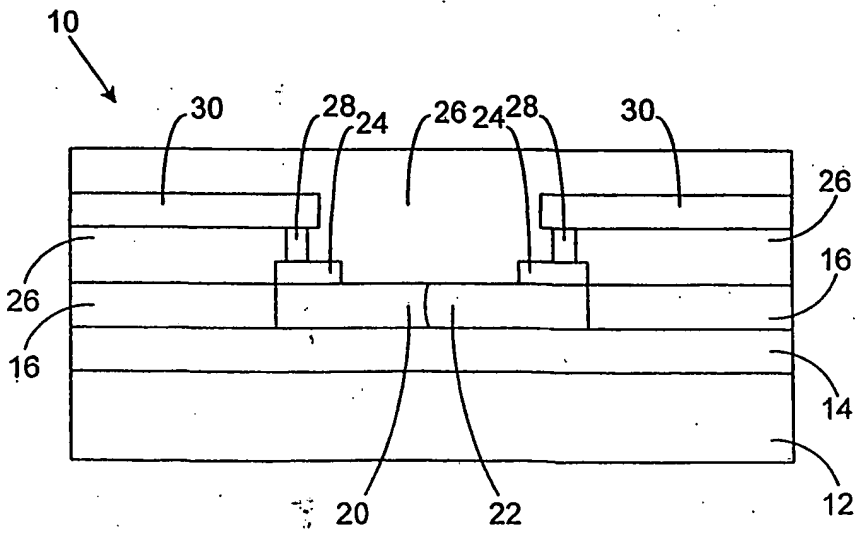

FIG. 3f